

# Curriculum Vitae

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## Personal Goal

I will contribute to computational science, engineering, and research in ways that have profound and global impact. I enjoy problem solving, especially the challenging problem of making a computational system faster and more reliable. For example, in both my masters and doctoral work, I approached high performance computing problems from a novel perspective that encompassed both hardware and software aspects of the system. In my postdoctoral research I focused on fault tolerance and performance of the Open MPI middle-ware software. At SiCortex I worked on improving their communications software to take advantage of the unique properties of the Kautz graph network topology. In summary, I want to continue to work on challenging and fulfilling problems at the state of the art.

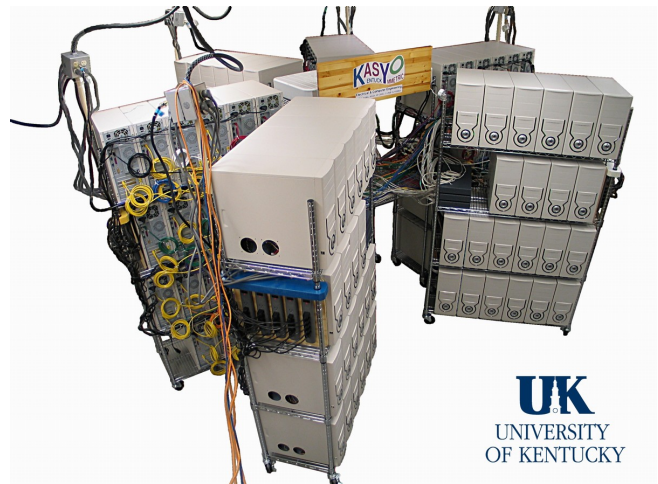
## Education

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| 2006 | Ph.D., Electrical and Computer Engineering, University of Kentucky<br>“Exploiting Sparseness of Communication Patterns for the Design of Networks in Massively Parallel Supercomputers”[4] |
| 1997 | M.S.E.E., Electrical and Computer Engineering, Purdue University<br>“Synchronous Aggregate Communication Architecture for MIMD Parallel Processing”[14]                                    |
| 1993 | B.S.C.E.E., Electrical and Computer Engineering, Purdue University   |

## Research Interests

- Simulations
- Parallel Processing
- Computer Architecture
- Parallel Operating Systems
- Beowulf/Parallel Computer Clusters
- High Speed Communication Networks
- High Performance Computing
- Fault Tolerance in HPC
- Scientific Computing
- Compilers

KASY0: 128 Node SFNN Cluster[6]



## Professional Experience

<i>2009-2009</i>	Technical Leader, Engineering, SPRTG Projects, Cisco Systems, Inc, San Jose, CA
<i>Spring 2009</i>	Communications and Kernel Developer, SiCortex, Inc, Maynard, MA
<i>2006-2009</i>	Research Associate, working on Open MPI in the Open Systems Lab Pervasive Technology Labs, Indiana University
<i>1999-2006</i>	Graduate Research Assistant, lead student researcher in the KAOS Lab Department of Electrical and Computer Engineering, University of Kentucky
<i>1994-2009</i>	Research Exhibitor/Presenter at the annual IEEE/ACM Supercomputing Conference Purdue University, University of Kentucky, Indiana University, and Cisco Systems, Inc.
<i>1996-1999</i>	Graduate Teaching Assistant, various graduate & undergraduate computer courses School of Electrical and Computer Engineering, Purdue University
<i>1994-1996</i>	Graduate Research Assistant, student researcher in the Parallel Processing Lab School of Electrical and Computer Engineering, Purdue University
<i>1992, 1993</i>	Summer Undergraduate Research Internship Engineering Research Center for Intelligent Manufacturing Systems, Purdue University

## Awards and Distinctions

<i>2000</i>	Gordon Bell Prize Honorable Mention, Price/Performance Category[9]
<i>2000</i>	SC2000 HPC Games, Most Innovative Hardware Prize (see KRAA Z-MP below)
<i>1997</i>	Magoon Award for Excellence in Teaching, Purdue University
<i>1989</i>	2nd place in Zoology at the 40th International Science and Engineering Fair “A Computer Simulation of Biological Evolution”

## Involvement in Open Source Projects

<i>Open MPI</i>	Developer and SVN Gatekeeper for the 1.2 and 1.3 release series <a href="http://www.open-mpi.org/">http://www.open-mpi.org/</a>
<i>Warewulf</i>	Contributor & Co-developer of the Warewulf cluster management suite 2003-2006 <a href="http://www.warewulf-cluster.org/">http://www.warewulf-cluster.org/</a>
<i>ATLAS</i>	Contributed a highly tuned Matrix Multiply routine for the Athlon+3DNow! architecture[12]
<i>AFAPI</i>	Co-developed the Aggregate Function API library[13] for parallel communications <a href="http://aggregate.org/AFAPI/">http://aggregate.org/AFAPI/</a>

## Computer Skills/Knowledge

<i>Languages</i>	Extensive experience with C, MPI, bash, Perl, and the GNU autoconf/automake/libtool suite. Also experienced with C++, MPL (MasPar's parallel C dialect), FORTRAN, Smalltalk, Pascal, VHDL, BASIC, Prolog, Lisp, and various assembly languages
<i>Networks</i>	Detailed knowledge of IPv4, TCP, UDP, Ethernet, and the Linux Kernel Networking code
<i>Tools+OS</i>	Expert user of subversion, mercurial, git, perceus, Linux and Mac OS X, and moderately skilled Linux administrator

## Clusters Facilitated via Design and Implementation (1994-2006)

KAOS Lab, Department of Electrical and Computer Engineering, University of Kentucky:

<i>KASY0</i>	128 AthlonXP Nodes, first Sparse Flat Neighborhood Network (SFNN)[6] First supercomputer to achieve under \$100/GFLOPS
<i>KLAT2</i>	64 Athlon Nodes, first Flat Neighborhood Network (FNN)[11, 10, 9] First supercomputer to achieve under \$1000/GFLOPS
<i>KRAA Z-MP</i>	12 Athlon Nodes, Aggregate Function Network (AFN) + FNN, demoed at SC2000
<i>Odie</i>	Four Athlon Nodes, AFN + Fast Ethernet, first cluster using Athlons, demoed at SC99
<i>Opus</i>	16 K6-2 Nodes + 16 CRT Video Wall, AFN + Fast Ethernet
<i>"Laptop cluster"</i>	9 (or 4) Athlon Laptop Nodes, LCD Video Wall, AFN + Fast Ethernet

Computational Fluid Dynamics Group, Department of Mechanical Engineering, University of Kentucky:

<i>KFC5</i>	48 Athlon64 Nodes, Gigabit Ethernet, tuned for lower power consumption
<i>KFC4</i>	56 AthlonXP Nodes, Fast Ethernet FNN + Gigabit Ethernet FNN
<i>KFC2</i>	48 AthlonXP Nodes, Channel Bonded Fast Ethernet
<i>KFC1</i>	20 dual AthlonMP Nodes, Channel Bonded Fast Ethernet

Electromagnetics Lab, Department of Electrical and Computer Engineering, University of Kentucky:

<i>KEMC</i>	24 Opteron Nodes + 15 LCD Panel Video Wall, Gigabit Ethernet
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Center for Radiophysics and Space Research, Department of Astronomy, Cornell University:

<i>"Harrington's"</i>	36 Opteron Nodes, Gigabit Ethernet FNN
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Comparative Planetology Laboratory, University of Louisville:

<i>COMPLINE</i>	40 AthlonXP Nodes, Fast Ethernet FNN
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Mechanical & Aerospace Engineering, Utah State University:

<i>FAUST</i>	64 AthlonXP Nodes, Fast Ethernet FNN
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Applied and Environmental Geophysics Research Group, Keele University, England:

<i>KAGe</i>	64 Athlon Nodes, Fast Ethernet FNN
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PAPERS Group, Parallel Processing Lab, School of Electrical and Computer Engineering, Purdue University:

<i>"32 cluster"</i>	32 PentiumII 300MHz Nodes + 6,400x4,800 pixel Video Wall, AFN + Fast Ethernet
<i>"Pentium cluster"</i>	Four Pentium 90MHz Nodes, AFN + 10 Mb/s Ethernet
<i>Spareparticus</i>	Eight 386DX33 Nodes + 2x4 CRT Video Wall, AFN + 10 Mb/s Ethernet
<i>Microcluster</i>	Four subnotebook 486SX16 Nodes, AFN without Ethernet
<i>"486 cluster"</i>	Four 486DX33 Nodes + 2x2 CRT Video Wall, Two AFNs[22, 23, 14] + 10 Mb/s Ethernet
<i>"First"</i>	Four 486DX2 66MHz Nodes, First prototype AFN[24] + 10 Mb/s Ethernet First Linux Cluster, Feb. 1994, <a href="http://aggregate.org/PurduePPL/first.html">http://aggregate.org/PurduePPL/first.html</a>

## List of Publications

For personal use, these publications can be downloaded from:

<http://homepage.mac.com/tmattox/publications/index.html>

- [1] Joshua Hursey, Timothy I. Mattox, and Andrew Lumsdaine. Interconnect agnostic checkpoint/restart in Open MPI. In *Proceedings of the Eighteenth International Symposium on High Performance Distributed Computing (HPDC 2009)*, pages 49–58. ACM, June 2009.
- [2] Timothy I. Mattox. Open MPI on Mac OS X: Enabling big science on the Mac. Scientific Development Poster presented during the Apple World Wide Developers Conference (WWDC07), San Francisco, California, June 2007.
- [3] Joshua Hursey, Jeffrey M. Squyres, Timothy I. Mattox, and Andrew Lumsdaine. The design and implementation of checkpoint/restart process fault tolerance for Open MPI. In *Proceedings of the 21st IEEE International Parallel and Distributed Processing Symposium (IPDPS)*. IEEE Computer Society, March 2007.
- [4] Timothy Ian Mattox. *Exploiting Sparseness of Communication Patterns for the Design of Networks in Massively Parallel Supercomputers*. PhD thesis, University of Kentucky, Lexington, Kentucky, June 2006.
- [5] Timothy E. Dowling, Mary E. Bradley, Edward Colón, John Kramer, Raymond P. LeBeau, Grace C.H. Lee, Timothy I. Mattox, Raul Morales-Juberías, Csaba J. Palotai, Vimal K. Parimi, and Adam P. Showman. The EPIC Atmospheric Model with an Isentropic/Terrain-Following Hybrid Vertical Coordinate. *Icarus*, 182(1):259–273, May 2006.
- [6] Timothy I. Mattox, Henry G. Dietz, and William R. Dieter. Sparse Flat Neighborhood Networks (SFNNs): Scalable Guaranteed Pairwise Bandwidth and Unit Latency. In *Proceedings of the Fifth Workshop on Massively Parallel Processing (WMPP'05) held in conjunction with the 19th IEEE International Parallel and Distributed Processing Symposium (IPDPS 2005)*, Denver, CO, USA, April 2005.
- [7] Th. Hauser, T.I. Mattox, R.P. LeBeau, H.G. Dietz, and P.G. Huang. Code optimizations for complex microprocessors applied to CFD software. *SIAM Journal on Scientific Computing*, 25(4):1461–1477, 2004.
- [8] H.G. Dietz and T.I. Mattox. Compiler optimizations using data compression to decrease address reference entropy. In Bill Pugh and Chau-Wen Tseng, editors, *Languages and Compilers for Parallel Computing, 15th International Workshop (LCPC 2002)*, volume 2481 of *Lecture Notes in Computer Science*, College Park, MD, USA, 2005. Springer-Verlag.
- [9] Th. Hauser, T.I. Mattox, R.P. LeBeau, H.G. Dietz, and P.G. Huang. High-Cost CFD on a Low-Cost Cluster. In *Proceedings of the IEEE/ACM SC2000 conference*, Dallas, TX, November 2000. Received Gordon Bell Prize Honorable Mention, Price/Performance category.
- [10] H.G. Dietz and T.I. Mattox. KLAT2's Flat Neighborhood Network. In *Proceedings of the 4th Annual Linux Showcase, Extreme Linux Track*, Atlanta, GA, October 2000.
- [11] H.G. Dietz and T.I. Mattox. Compiler Techniques For Flat Neighborhood Networks. In S.P. Midkiff, J.E. Moreira, M. Gupta, S. Chatterjee, J. Ferrante, J. Prins, W. Pugh, and C.-W. Tseng, editors, *Languages and Compilers for Parallel Computing, 13th International Workshop (LCPC 2000)*, volume 2017 of *Lecture Notes in Computer Science*, pages 244–259, IBM Watson Research Center, Yorktown, NY, 2001. Springer-Verlag.
- [12] Hank Dietz and Tim Mattox. Inside the KLAT2 Supercomputer: The Flat Neighborhood Network and 3DNow! <http://arstechnica.com/cpu/2q00/klat2/klat2-1.html>, June 2000.
- [13] H.G. Dietz, T.I. Mattox, and G. Krishnamurthy. The Aggregate Function API: It's not just for PAPERS anymore. In Z. Li, P.-C. Yew, S. Chatterjee, C.-H. Huang, P. Sadayappan, and D. Sehr, editors, *Languages and Compilers for Parallel Computing, 10th International Workshop (LPCP'97)*, volume 1366 of *Lecture Notes in Computer Science*, pages 277–291, Minneapolis, MN, 1998. Springer-Verlag.
- [14] Timothy I. Mattox. Synchronous aggregate communication architecture for MIMD parallel processing. Master's thesis, School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN, August 1997.

- [15] H.G. Dietz and T.I. Mattox. Managing polyatomic coherence and races with replicated shared memory. *IEEE Computer Society Technical Committee on Computer Architecture (TCCA) Newsletter*, pages 53–58, March 1997.
- [16] R. Hoare, T.I. Mattox, and H. Dietz. TTL-PAPERS 960801: The Modularly Scalable, Field Upgradable, Implementation of Purdue’s Adapter for Parallel Execution and Rapid Synchronization. Technical Report <http://aggregate.org/AFN/960801/Index.html>, School of Electrical Engineering, Purdue University, West Lafayette, IN, 1997.
- [17] R. Hoare, H. Dietz, T. Mattox, and S. Kim. Bitwise aggregate networks. In *Proceedings of The Eighth IEEE Symposium on Parallel and Distributed Processing (SPDP ’96)*, New Orleans, LA, October 1996.
- [18] H.G. Dietz, R. Hoare, and T. Mattox. A fine-grain parallel architecture based on barrier synchronization. In A. Reeves, editor, *1996 International Conference on Parallel Processing*, volume I Architecture, pages 247–250, Bloomington, IL, August 1996. IEEE Computer Society Press.
- [19] Henry G. Dietz, T. M. Chung, and Timothy I. Mattox. A parallel processing support library based on synchronized aggregate communication. In C.-H. Huang, P. Sadayappan, U. Banerjee, D. Gelernter, A. Nicolau, and D. Padua, editors, *Languages and Compilers for Parallel Computing, 8th International Workshop (LCPC’95)*, volume 1033 of *Lecture Notes in Computer Science*, pages 254–268, Columbus, OH, USA, 1996. Springer-Verlag.
- [20] H.G. Dietz, T.M. Chung, T. Mattox, and T. Muhammad. A synchronization and aggregate communication library for PAPERS clusters. Technical Report <http://aggregate.org/TechPub/TR19950131/tr950131.html>, School of Electrical Engineering, Purdue University, West Lafayette, IN, January 1995.
- [21] H.G. Dietz, T.M. Chung, T.I. Mattox, and T. Muhammad. Purdue’s Adapter for Parallel Execution and Rapid Synchronization: The TTL-PAPERS Design. Technical Report <http://aggregate.org/TechPub/ICPP95/icpp95.html>, School of Electrical Engineering, Purdue University, West Lafayette, IN, January 1995.
- [22] H.G. Dietz, T. Muhammad, and T. Mattox. TTL Implementation of Purdue’s Adapter for Parallel Execution and Rapid Synchronization. Technical Report <http://aggregate.org/TechPub/super4.pdf>, School of Electrical Engineering, Purdue University, West Lafayette, IN, December 1994.
- [23] Henry G. Dietz, William E. Cohen, T. Muhammad, and Timothy I. Mattox. Compiler techniques for fine-grain execution on workstation clusters using PAPERS. In K. Pingali, U. Banerjee, D. Gelernter, A. Nicolau, and D.A. Padua, editors, *Languages and Compilers for Parallel Computing, 7th International Workshop (LCPC’94)*, volume 892 of *Lecture Notes in Computer Science*, pages 31–45, Ithaca, NY, 1995. Springer-Verlag.
- [24] H.G. Dietz, T. Muhammad, J.B. Sponaugle, and T. Mattox. PAPERS: Purdue’s Adapter for Parallel Execution and Rapid Synchronization. Technical Report TR-EE 94-11, School of Electrical Engineering, Purdue University, West Lafayette, IN, USA, March 1994.