

CHASE TSANG

(Address removed in online version)

chaset@mac.com

CAREER SUMMARY

Highly effective Hardware Engineer with extensive experience in design and verification of high-speed digital and mixed-signal circuits in the automated test equipment industry. Knowledgeable in related issues such as testability and reliability as well as documentation and support issues. Established ability to manage projects, deliver on time, and work with diverse teams. Proven excellence in problem solving, communication, and flexibility. Described as "Plug and Play Engineer" due to ability to be immediately effective and successful in any new role. Bilingual in Japanese and English.

TECHNICAL SKILLS/KNOWLEDGE

Design Tools:	Cadence Allegro Design Entry, Xilinx ISE, SPICE, Verilog, waveform viewers
Programming Languages:	C++, Visual Basic, Perl, Shell scripting
Software Development:	Visual Studio, Rational ClearQuest, Rational ClearCase
Project Management:	Microsoft Project, Primavera Enterprise
Office Productivity:	Microsoft Word, Excel, PowerPoint, Visio
Operating Systems:	Unix and Unix-like operating systems, Macintosh, OS X, MS-DOS/Windows
Other:	HTML, SQL, Working knowledge of electronic laboratory equipment, including GPIB control, Teradyne IG-XL for Flex/UltraFlex/J750 (control software for test systems)

PROFESSIONAL EXPERIENCE

TERADYNE JAPAN BUSINESS UNIT, Kumamoto, Japan

2006 – 2009

Development Engineer

Oversaw design, layout, testing, and verification of several key components of complex ATE systems including PCBs and FPGAs.

- Managed a team and led the redesign of a key instrument for the IP750Ex image sensor test system, including component selection, schematics entry, and layout supervision that was delivered on-target despite extremely compressed schedule. This instrument is capable of simultaneously capturing 4 data streams to be sent to the DSP engine for processing, making the IP750Ex the leading system in the industry for parallel testing of CCD image sensors.
- Developed calibration and verification suite for a new high-voltage instrument for the Flex platform using Visual Basic and completed 2.5 months ahead of schedule. Hence the instrument met the release target, allowing Teradyne Japan to secure orders for dozens of instruments even during the critical downturn in orders.
- Averted an expensive field retrofit by discovering a latent bug before shipment to customers through developing and executing design verification on the instrument and implementing a creative method for measuring instrument timing accuracy.
- Developed a cable interface for the IP750Ex test system, which came in 10% under the cost goal and met the delivery target date.

TERADYNE JAPAN BUSINESS UNIT (Continued)

- Developed and executed verification test for InfiniBand interface implemented on the Virtex4 platform. Wrote custom software to manipulate control registers in the RocketIO interface via the embedded PowerPC processor in order to measure effects of various settings on transmission errors.

TERADYNE, INC., SEMICONDUCTOR TEST DIVISION, Agoura Hills, CA**1997 – 2006****Test Development Engineer**

2003 – 2006

Designed and implemented production tests and test processes for new products introduction. Tracked process capability data generated by these tests.

- Increased profit margins on an existing product by revealing additional design margin via production test. Created performance verification software using C++ and developed processes for use. Developed SQL queries to analyze production data, which showed better than expected margin and allowed Teradyne to market the higher performance as a competitive feature.
- Mentored 2 junior engineers for 2 + years allowing them to maintain the test software and procedures as well as develop new ones for later products.

Development Engineer

1997 – 2003

Executed the design, layout, testing, verification and maintenance engineering of PCBs. ASIC design verification and yield improvement.

- Prevented test escapes that could cost millions of dollars in wasted NRE (non recurring expense) by developing test programs for unit testing of a timing generator / formatter ASIC.
- Designed the central control board prototype that was the basis for the central control board in Teradyne's flagship UltraFlex platform, resulting in a standardized design that formed a basis for several subsequent designs for engineering and production use.
- Eliminated costs associated with scrapping faulty PCBs due to ASIC failure by carrying out several bench tests to identify the nature of failures, and by modifying an engineering test bed system to allow further screening. The Quality Improvement Team was recognized at a companywide awards ceremony for this achievement.

Earlier Work – Miscellaneous implementation and verification of design modifications for the J973 test system, design of analog filter board for the J973 Mixed Signal Option.

EDUCATION

MS, Electrical Engineering, University of Southern California, Los Angeles, CA

BS, Engineering, Social science concentration in psychology, Harvey Mudd College, Claremont, CA

Tau Beta Pi